

IN THE CLAIMS:

1-15. canceled

16. (previously presented) A method of fabricating a non-volatile memory transistor comprising the steps of:
preparing a semiconductor substrate;
forming a gate stack on the substrate, as follows:
depositing a single layer of high-k dielectric material, without an underlying oxide insulator layer and an overlying oxide insulator layer;
exposing the high-k dielectric material to an ionized species;
in response to the ionized species exposure, inducing trapping centers in the high-k dielectric material; and
forming an electrode layer overlying the high-k dielectric with the charge trapping centers; and
forming drain and source regions on opposite sides of the gate stack.

17. (original) A method as in claim 16 wherein the high-k dielectric material comprises at least one of aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), zirconium oxide (ZrO_2), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), cesium oxide (CeO_2), lanthanum oxide (La_2O_3), tungsten oxide (WO_3), yttrium oxide (Y_2O_3), bismuth silicon oxide ($\text{Bi}_4\text{Si}_2\text{O}_{12}$), barium strontium oxide ($\text{Ba}_{1-x}\text{Sr}_x\text{O}_3$), lanthanum aluminum oxide (LaAlO_3), hafnium silicate (HfSiO_4), zirconium silicate (ZrSiO_4), aluminum hafnium oxide (AlHfO), aluminum oxynitride (AlON), hafnium

silicon oxynitride (HfSiON), zirconium silicon oxynitride (ZrSiON), barium titanate (BaTiO_3), strontium titanate (SrTiO_3), lead titanate (PbTiO_3), barium strontium titanate (BST) ($\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$), lead zirconium titanate, lead lanthanum titanate, bismuth titanate, strontium titanate, lead zirconium titanate (PZT ($\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$)) barium zirconium titanate, strontium bismuth tantalate, lead zirconate (PbZrO_3), PZN ($\text{PbZn}_x\text{Nb}_{1-x}\text{O}_3$), PST ($\text{PbSc}_x\text{Ta}_{1-x}\text{O}_3$), or PMN ($\text{PbMg}_x\text{Nb}_{1-x}\text{O}_3$).

18-19. canceled

20. (previously presented) A method as in claim 16 wherein exposing the high-k dielectric material to the ionized species includes exposing the high-k dielectric to a species selected from the group consisting of oxygen, nitrogen, and hydrogen.

21. (previously presented) A method as in claim 16 wherein exposing the high-k dielectric material to the ionized species includes exposing the high-k dielectric material to a plasma for an exposure time in the range of about 10 seconds and 100 seconds.

22. (previously presented) A method as in claim 16 wherein depositing the high-k dielectric material includes depositing using an ALD method.

23. (previously presented) A method as in claim 16 further comprising a densification anneal step after the deposition of the high-k dielectric material.

24. (original) A method as in claim 16 wherein the formation of the drain and source regions comprises an angle source and drain implantation.

25. (previously presented) A method as in claim 16 wherein the semiconductor substrate is selected from a group consisting of SOI substrate, bulk silicon substrate, and insulator substrate.

26. (original) A method as in claim 16 wherein the memory transistor is a multi-bit memory transistor.

27. (previously presented) A method as in claim 16 wherein exposing the high-k dielectric material to an ionized species includes using an ion energy in the range of about 10 to 300 keV and a dose in the range of about 1×10^{14} to 1×10^{17} .

28. (previously presented) A method as in claim 16 wherein exposing the high-k dielectric material to an ionized species includes generating a plasma using an inductively coupled plasma (ICP) source.